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Inhomogeneous Carrier Transport at Contact/GaN Interfaces and Thermal Instability of Vertical Light-Emitting Diodes

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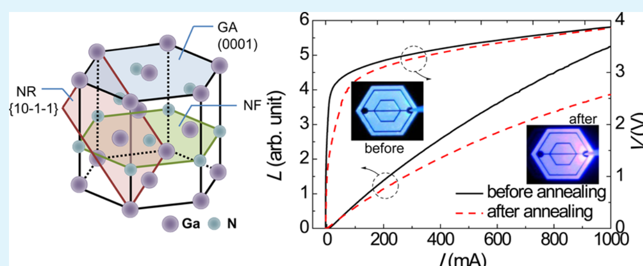
ABSTRACT: The carrier-transport behavior at the interface of a contact and n-type GaN was investigated for group III nitride vertical light-emitting diodes (LEDs). Three types of samples were investigated including dry-etched flat Ga-polar n-GaN (GA), dry-etched flat N-polar n-GaN (NF), and wet-etched roughened N-polar n-GaN (NR). Schottky diodes fabricated using a palladium contact revealed that carrier transport at the contact/GaN interface could be understood in terms of the barrier inhomogeneity model, in which the local shallow barriers dominated the overall carrier transport. Kelvin probe force microscopy showed that the peculiar crystallographic structures and native defects (acting as the local shallow barriers) led to the largest tunneling probability of the NR samples. The study was followed up by forming a TiN/Al contact on the NR surfaces to study the thermal instability of the vertical LEDs, revealing that the vertical LEDs were degraded after a thermal annealing process. This could be related to the n-contact size, indicating that the degradation of vertical LEDs was likely due to the failure of Ohmic patches (contacts formed on the defects and/or the tip/edge of hexagonal cones) at elevated temperature.



KEYWORDS: *carrier transport, contact, GaN, Ohmic, N-polar, vertical light-emitting diodes*

1. INTRODUCTION

Group III nitride light-emitting diodes (LEDs) have undergone rapid development because of their great potential for application in future solid-state lighting technology.[1−4] Rapid development of LED technology with improved luminous efficiency was possible because of novel epitaxial design/growth,[5−7] effective suppression of charge separation[6,7] and efficiency droop,[8,9] advanced fabrication processes,[10−16] and improved packaging technologies.[17] One of the recently developed innovative fabrication technologies is the so-called vertical LED process,[18−22] which can be achieved via process combination of wafer bonding (or electroplating) and laser lift-off (LLO) techniques. Indeed, the vertical LED process provided a new way to obtain high-power and high-efficiency LEDs because it exhibits low series resistance in devices associated with uniform current spreading, enhanced extraction efficiency, and excellent heat dissipation capability.

However, vertical LEDs still suffer from low process yield and thermal instability, causing them to be highly expensive in practice. This is related to the complicated vertical process involving the physical removal of insulating sapphire substrates from nitride thin films using the LLO technique and wafer bonding. For example, after removal of the sapphire substrate, the remaining nitride thin films may contain a large number of surface states, crystallographic defects, and macroscopic cracks.[23] More importantly, the exposed GaN plane upon sapphire removal is a nitrogen (N)-terminated GaN surface, i.e., N-polar GaN plane, on which an n-type Ohmic contact should be formed for the fabrication of LED devices. Previously, it was shown that the impurity concentration,[24] surface states,[25,26] contact properties,[26−33] structural stability,[34] and chemical inertness to solutions[35] of the N-polar plane are quite different from those of gallium (Ga)-terminated or Ga-polar GaN planes. One of the primary reasons for these different properties of the N-polar plane compared to the Ga-polar one is the crystallographic orientation of Ga−N bonds, which leads to oppositely directed internal spontaneous polarization fields (P_{SP}).

There are two primary issues to resolve regarding the fabrication of highly efficient and reliable vertical LEDs: first, a thermally stable Ohmic contact is to be formed on the N-polar n-GaN; second, robust surface textures should be formed on top of the n-GaN layer. In pursuit of the latter, a large number of groups have investigated distinctive surface textures to maximize the light extraction efficiency of LEDs, including the generation of a crystallographic hexagonal cone structure by wet etching,[20,36] the formation of fine surface textures by dry etching[37] and/or nanostructure deposition,[38] the use of graded

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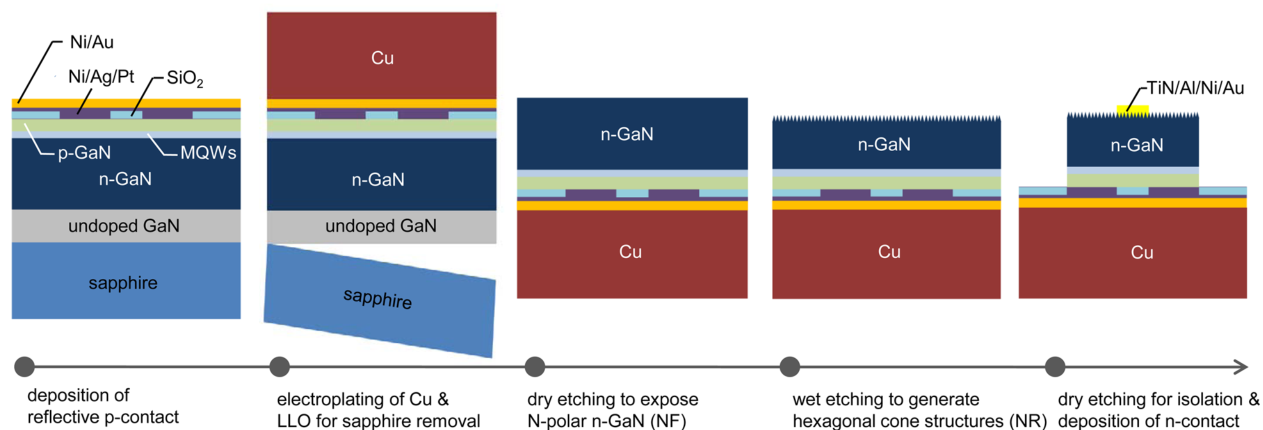

Figure 1. Schematic process flow for the fabrication of vertical LEDs.

refractive index layers,[39] microlens array,[40,41] patterning by self-assembled lithography,[42] nanopyramid,[43] and concave micro-structures.[44,45] Among these techniques, the wet-etching technique is most widely and practically used because it can easily produce excellent surface textures with a high density of hexagonal cones exceeding $\sim 10^8$ cm^{-3}. Indeed, the capability of wet etching on the N-polar surface, which is possible because of the favorable direction of internal spontaneous polarization P_{SP}, is one of the successes in the fabrication of highly efficient vertical LEDs, as will be discussed later.

Regarding the metal contact with N-polar n-GaN, carrier-transport behavior and contact issues have also been reported by several groups.[26−33] Notably, one of the commonly observed findings is the thermal instability of the Ohmic contact formed on the N-polar n-GaN, leading to thermal degradation of vertical LEDs. This was explained in terms of the formation of an interfacial AlN/GaN structure after thermal annealing of a titanium (Ti)/aluminum (Al)-based contact, in which the presence of P_{SP} prevented the accumulation of electrons at the interface, resulting in a large interfacial AlN barrier that impedes carrier transport.[27,28] In addition, the generation of acceptor-like defects associated with the out-diffusion of Ga atoms was also reported to compensate for the majority carriers and hence the degradation of Ohmic contact.[26,29,30] However, there is a need for in-depth comprehensive studies on the carrier-transport mechanism and thermal instability of the N-polar contact and its influence on the performance characteristics of vertical LEDs. More specifically, while the properties of the contacts formed on the wet-etched roughened N-polar n-GaN (referred to herein as "NR"), dry-etched flat N-polar n-GaN ("NF"), and dry-etched flat Ga-polar n-GaN ("GA") are of particular interest for understanding the exact mechanism of carrier transport, comprehensive contact studies of these three different planes with a reasonable model are very rare. In this regard, we investigated the electrical characteristics and carrier-transport mechanisms of metal contacts formed on three relevant n-GaN planes, GA, NF, and NR, and then elucidated the thermal degradation mechanism of the vertical LEDs associated with the contact issues.

2. EXPERIMENTAL SECTION

The present contact study used commercially available LED wafers grown on an insulating sapphire substrate. The LED structures consisted of 2.0-μm-thick undoped GaN, 4.0-μm-thick silicon (Si)-doped n-GaN, a 0.1-μm-thick multiple quantum-well active region, a p-AlGaN-based electron blocking layer, and $\sim$0.10-μm-thick magnesium (Mg)-doped p-GaN. The peak emission wavelength was around 450 nm. For a comparative study on the three different n-GaN planes, first, the GA sample was prepared by dry-etching the top layers of the LED wafers to a thickness of 1.0 μm using an inductively coupled plasma reactive ion etching (ICPRIE) system, resulting in exposure of the flat (0001) Ga-polar n-GaN surface. To fabricate the N-polar samples and to complete vertical LEDs, the LED wafers were processed as shown in Figure 1. For example, (1) the SiO_2 films were deposited on top of the p-GaN layer using a plasma-enhanced chemical vapor deposition system, (2) the SiO_2 films were patterned using conventional photolithographic techniques and wet etching by a buffered oxide etchant in order to define the current blocking layer, (3) the nickel (Ni, $\sim$1 nm)/silver (Ag, 200 nm)/platinum (Pt, 30 nm) reflective p-contact scheme was deposited onto the exposed top p-GaN layer using an e-beam evaporator, followed by rapid thermal annealing at 480 °C for 1 min in an N_2 ambient atmosphere in order to form a p-type Ohmic contact, (4) the entire wafer was coated using the Ni/gold (Au) scheme, on which the copper (Cu) layer was electroplated as the host substrate, (5) the LLO process was performed to separate the sapphire substrate from the LED films by irradiating with a 248 nm pulsed laser (KrF excimer), (6) the separated surface of the LED films was cleaned with a HCl/deionized water (1:2) solution in order to remove the Ga droplets, followed by dry etching to a thickness of 3.5 μm in order to expose the N-polar n-GaN, namely, the completion of sample NF, (7) the dry-etched N-polar surface was further wet-etched using a 2 M KOH solution in order to generate hexagonal cone structures (the completion of sample NR), and (8) for isolation of an LED chip, dry etching was performed using ICPRIE, followed by the formation of a TiN (10 nm)/Al ($\sim$2.0 μm)/Ni (200 nm)/Au (400 nm) Ohmic contact on the textured N-polar n-GaN surfaces.[30]

The surfaces of the GA, NF, and NR samples were observed by atomic force microscopy (AFM) and Kelvin probe force microscopy (KPFM). The KPFM measurement was performed using a Nanoscope IV multimode AFM system with a curvature radius of <30 nm. The first scan was made in tapping mode in order to obtain the surface morphology; a second scan was performed in lift mode at a constant tip−surface separation of <100 nm and a bias of 5 V in order to measure the surface potentials. Hall effect measurements were also performed for sample GA in order to measure the electron concentration (N = 9.0 × 10^{18} cm^{-3}) and the Hall mobility (190 cm^2 V^{-1} s^{-1}). The measured N value was higher than the initial Si doping concentration ($\sim$5 × 10^{18} cm^{-3}), which is attributed to the generation of plasma-induced donor-like surface defects such as nitrogen vacancies (V_N) and oxygen impurities (O_N). To understand the carrier-transport mechanism, Schottky diodes were fabricated on the sample surfaces using a standard photolithographic technique and metal deposition by an e-beam evaporator (see the inset of Figure 3). For example, chromium (Cr)/Au (30 nm/100 nm) and palladium (Pd, 100 nm) layers were used as the Ohmic contact (surrounding

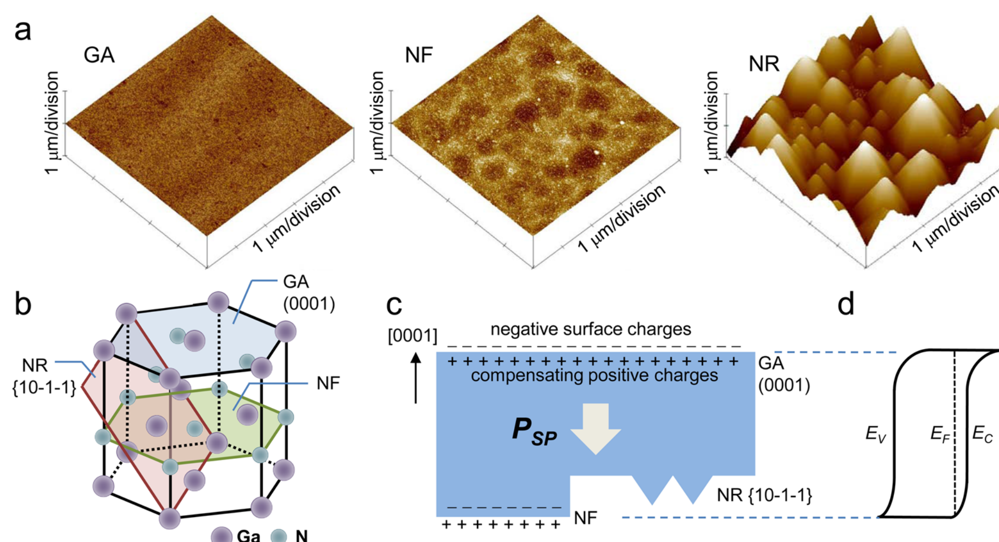

Figure 2. (a) 5 × 5 AFM surface images of the GA, NF, and NR samples. (b) Schematic illustrations of GA, NF, and NR planes in the wurtzite structure. Schematics of (c) P_{SP} and (d) energy band diagrams depending on the plane.

region) and Schottky contact (central circle), respectively. The diameter (d) of the Schottky contact was varied over a range of 30−500 μm. Note that buffered oxide etchant and deionized water were used to clean the sample surface prior to metal deposition. A transmission line model (TLM) method was used to evaluate the contact resistance and Ohmic behavior.[34] The electrical and optical characteristics of the contacts and LEDs were measured using a parameter analyzer (HP4156A) connected to the photodiode.

3. RESULTS AND DISCUSSION

Figure 2a shows the 5 × 5 AFM surface images of the GA, NF, and NR samples. It is shown that the surfaces of GA and NF are relatively flat and smooth, while that of NR is quite rough because of an exposed crystallographic plane of {10−1−1}, as illustrated in the wurtzite structure of Figure 2b. As mentioned above, the feasible wet etching of the NF sample against the GA sample is due to the favorable direction of internal P_{SP} built from the Ga-polar plane to the N-polar plane, as shown in Figure 2c. For example, under the presence of P_{SP}, the N-polar plane would be positively charged because of the hole flow to the N-polar side and subsequent trapping at the surface states. In this case, the hydroxide ions (OH^-) in alkali solutions, which are the key species for the wet-etching process,[35] can access the N-polar plane, and thereby the wet etching can proceed with the oxidation of GaN and subsequent dissolution of gallium oxide. In contrast, the Ga-polar plane cannot be wet-etched because the negatively charged surfaces prevent hydroxide ions from accessing the GaN surface.

In addition to wet etching, the presence of P_{SP} can also affect the surface band bending, as shown in Figure 2d. For example, the negative surface charges of the Ga-polar plane will induce compensating positive charges near the GaN surface, leading to upward surface band bending. In contrast, P_{SP} induces positive surface charges at the N-polar planes, leading to an accumulation of compensating positive charges and hence downward surface band bending. As a result, the energy band diagram can be drawn as shown in Figure 2d. For the NR samples consisting of several semipolar {10−1−1} planes, the effect of P_{SP} can be somewhat reduced depending on the vector sum of the tetrahedral bonds.[33] On the basis of the degree of surface band bending, Ohmic contact to the Ga-polar n-GaN (GA sample) is expected to be difficult to obtain, while that to the N-polar GaN (NF and NR samples) would be relatively easier because the Schottky barrier height (Φ_B) at the contact/GaN interface is theoretically expected to form.

$$\Phi_{B,NF} < \Phi_{B,NR} < \Phi_{B,GA} \quad (1)$$

To investigate the actual Φ_B and carrier-transport behavior, the Schottky diodes were fabricated on three different planes using a Pd contact, as shown in the inset of Figure 3. The

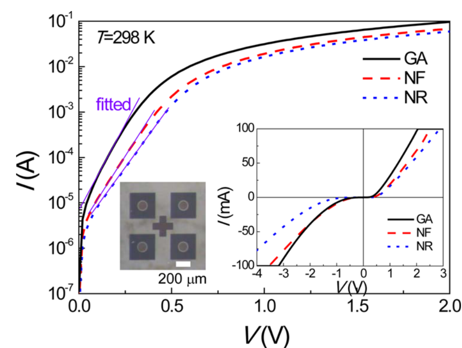

Figure 3. Semilogarithmic forward $I-V$ curves of Schottky diodes formed on the GA, NF, and NR samples. The left and right insets show the optical microscopic top view of fabricated Schottky diodes (d = 100 μm) and the $I-V$ characteristics of the diodes, respectively.

diameter of the Schottky contact was 100 μm. It was confirmed from the TLM measurement that a Cr/Au Ohmic contact could be formed on all three planes with a specific contact resistance (ρ_{sc}) of ~10^{-4} Ω·cm^2 (not shown). Figure 3 shows the semilogarithmic forward current−voltage ($I-V$) curves of Schottky diodes formed on the GA, NF, and NR samples. The inset of Figure 3 shows the $I-V$ characteristics, demonstrating the poor rectifying behavior of the samples; e.g., the rectification ratio measured at ±1 was as low as ~50.

According to Padovani and Stratton,[46,47] the carrier transport at a contact/semiconductor can be explained by thermionic emission (TE), thermionic field emission (TFE), and field emission (FE) models depending on the temperature (T) and carrier concentration (N), i.e., $kT/qE_{00} \gg 1$ for TE, kT/qE_{00} ~

1 for TFE, and $kT/qE_{00} \ll 1$ for FE, where k is the Boltzmann constant, q is the electron charge, and E_{00} is the tunneling parameter. Here, E_{00} is given by

$$E_{00} = \frac{qh}{4\pi}\left(\frac{N}{\varepsilon_s m^*}\right)^{1/2} \quad (2)$$

where h is the Planck constant, ε_s is the dielectric constant of GaN ($\varepsilon_s = 8.9\varepsilon_0$), and m^* is the electron effective mass ($m^* = 0.2m_e$). When $N = 9.0 \times 10^{18}$ cm^{-3} and $T = 298$ K are applied and eq 2 is used, the kT/qE_{00} value is calculated to be 0.62, which lies in the regime of TFE, i.e.,[46−48]

$$I = A\frac{A^{**}T\sqrt{\pi E_{00}e(\Phi_B - V - \xi)}}{k\cosh(E_{00}/kT)}\exp\left[-\frac{e\xi}{kT} - \frac{q}{E_{00}\coth(E_{00}/kT)}(\Phi_B - \xi)\right]\exp\left[\frac{qV}{E_{00}\coth(E_{00}/kT)}\right] \quad (3)$$

where A is the area of the Schottky contact, A^{**} is the Richardson constant (26.4 A cm^{-2} K^{-2}),[49] and ξ is the energy difference between the conduction band edge (E_C) and the Fermi level (E_F).

Table 1 summarizes the Schottky parameters including Φ_B, E_{00}, the ideality factor (n), and N as obtained by theoretical fits

Table 1. Schottky Parameters of All Diodes Measured at 298 K (d = 100 μm)

	Schottky parameters			
sample	Φ_B (eV)	E_{00} (meV)	n	N ($\times 10^{19}$ cm^{-3})
GA	1.15	52	2.1	1.4
NF	1.32	106	4.1	5.8
NR	1.52	113	4.4	6.6

of forward $I-V$ curves using eq 3. Theoretical fitting was performed using commercialized software (Microcal *Origin 6.0*), which presented excellent fits in the specific low-voltage ranges (see the fitting results as indicated by lines in Figure 3); i.e., the goodness of fit was as high as 0.998. The ideality factor n was calculated using the relationship $n = E_{00}/kT \coth(E_{00}/kT)$, and N was estimated from eq 2. Notably, unlike the theoretical prediction, the actual Φ_B of the NR sample was highest, while that of the GA samples was lowest, as follows:

$$\Phi_{B,GA} < \Phi_{B,NF} < \Phi_{B,NR} \quad (4)$$

This finding indicates that carrier transport at the contact/GaN interface cannot be simply explained in terms of the surface band bending effect associated with the polarization field P_{SP} and charge traps. This hypothesis is further supported by the obtained large n values of 2.1−4.4, implying that Schottky diodes experienced nonideal carrier transport at the contact/GaN interface. As a possible origin of the large n value, conventionally, the presence of surface states associated with crystallographic defects, such as threading dislocations and point defects, a series resistance, and a generation−recombination current within the space charge region, was suggested.[46−48,50−52] However, the effect of a series resistance is ignored because the electrical resistivities of n-GaN and the Ohmic contact are very low. In addition, the effect of the generation−recombination current can also be neglected because of the nature of a wide-band-gap semiconductor (E_g = 3.4 eV). Thereby, the presence of surface states associated with the crystallographic defects is typically regarded as the primary reason for anomalous carrier transport at the contact/GaN interface.

Another important finding shown in Table 1 is the large E_{00} values of all samples, indicating that carrier transport is predominated by tunneling. Note that the N values estimated from E_{00} were even larger than the initial carrier concentration (9.0×10^{18} cm^{-3}), as measured by the Hall effect measurement. Considering that the $I-V$ method yields a higher surface-sensitive carrier concentration of the samples (because carrier transport is mainly involved at the contact/GaN interface), this constitutes essential proof that all samples contained substantial donor-like surface defects, which is in good agreement with previous reports.[48,50,53] For our samples, it is predictable that the GA and NF samples may contain a number of donor-like surface defects such as V_N and O_N due to plasma exposure of the sample under dry etching. For the NR sample, however, the surface is expected to have much fewer donor-like defects because of the possible removal of a damaged layer by subsequent wet etching. However, interestingly, the NR sample showed the largest E_{00} value among the samples. This indicates that additional correlations other than the effect of plasma-induced donor-like surface defects may appear.

So far, carrier transport at contact/GaN interfaces was analyzed using the TFE model, in which the Schottky barrier is assumed to be homogeneous. However, recent studies revealed that carrier transport at the contact/GaN interface is further influenced by the statistical distribution of the inhomogeneous barriers, which has a Gaussian distribution with a mean barrier height and standard deviation.[46,47,54−59] In this regard, we also investigated the effect of barrier inhomogeneity in our samples; namely, the area dependence of diodes was investigated as shown in Figure 4. Figure 4a shows typical $I-V$ curves of Schottky diodes fabricated on the NR sample as a function of the contact diameter d. It is evident that the $I-V$ curves are significantly dependent on the contact size (the same behavior was also observed for the GA and NF samples, not shown here). Figure 4b shows the reverse leakage current (I_R) measured at −1.0 V for all samples plotted as a function of d. Note that I_R increases with the contact area A, e.g., $I_{R_GA} \propto d^{1.89}$, $I_{R_NF} \propto d^{2.15}$, and $I_{R_NR} \propto d^{2.07}$. This indicates that the leakage current is due to the randomly distributed bulk defects against the surface leakage origins.[53] Accordingly, Φ_B was also shown to be negatively correlated with d and A, i.e., the larger A is, the lower Φ_B is (see Figure 4c). This is quite feasible considering that the randomly distributed bulk defects would have a lower barrier height than the remaining sound region.

The origins of distributed bulk leakage that have a locally shallow barrier may be due to crystallographic defects such as dislocations, stacking faults, point defects, and/or the specific crystallographic planes/structures in the NR samples. To investigate direct evidence of inhomogeneous barriers, AFM and KPFM measurements were performed as shown in Figure 5. Parts a−c of Figure 5 show the 5 × 5 μm^2 surface morphology, and parts d−f of Figure 5 show the corresponding surface contact potential (V_{cp}) images of the GA, NF, and NR samples, obtained by AFM and KPFM, respectively. The statistical distributions of the feature height (obtained by AFM) and surface contact potential (obtained by KPFM) are also shown in Figure 5. Note that the surface of the NR sample is

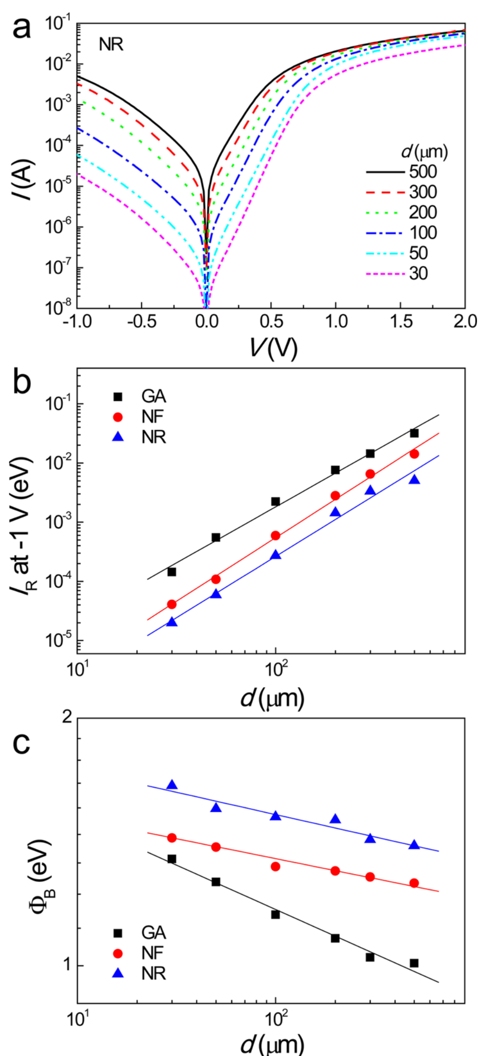

Figure 4. (a) Typical $I-V$ curves of the Schottky diodes fabricated on the NR sample as a function of the contact diameter d. (b) Reverse leakage current (I_R) measured at −1.0 V. (c) Φ_B values of all samples plotted as a function of d.

quite rough, that of the NF sample is intermediate, and that of the GA sample is very smooth, with root-mean-square (rms) surface roughness values of 0.7, 12.5, and 204.5 nm, respectively. As expected, the roughness of the NR sample was due to the exposure of a hexagonal cone structure by wet etching. However, despite the same dry etching condition as that used for the preparation of the GA and NF samples from an identical wafer, the greater surface roughness of the NF sample than that of the GA sample might be due to the combined effects of LLO-induced surface undulation[60] (associated with the formation and removal of gallium droplets) and/or different etching kinetics depending on polarity.[34]

While AFM observations showed large differences in the rms surface roughness depending on the sample, the KPFM measurements exhibited less difference in the rms V_{cp} roughness, as shown in Figure 5d−f (compare the line widths of the distributions). According to the theory of KPFM, the measured V_{cp} represents the difference in the work function between a conducting AFM tip and the GaN surface, i.e.,[61]

$$V_{cp} = \frac{\Phi_{GaN} - \Phi_{tip}}{q} \tag{5}$$

where Φ_{GaN} and Φ_{tip} are the work functions of the GaN surface and tip, respectively. Considering that the tip is coated with Pt, i.e., Φ_{tip} = 5.65 eV, the measured V_{cp} mapping is considered to be a measure of the variation in the work function of GaN (Φ_{GaN}). Therefore, a significant deviation in the rms V_{cp} roughness from the rms surface roughness indicates that inhomogeneous barriers are less influenced by the geometrical effect associated with the surface roughness but more influenced by native defects. On the other hand, the NR sample showed a quite large V_{cp} roughness, which cannot be explained solely by the effect of native defects. Indeed, Figure 5f shows that V_{cp} fluctuates noticeably near the top angular point and edge region of the hexagonal cones, indicating a combined effect of native defects and geometrical surface roughness. Unfortunately, a more detailed analysis was unavailable for the NR sample because of the extreme surface roughness, which disrupted the AFM tip during a line-by-line scan.

Figure 6 summarizes the rms surface roughness, V_{cp} roughness, and E_{00} values of all samples. It is evident that the E_{00} values show nearly the same sample dependence with the rms roughness, particularly for the rms V_{cp} roughness. This indicates that the strong tunneling at the contact/GaN interface primarily originates from the fluctuating barriers associated with native defects and specific surface structures, although other factors, e.g., local enhancement of the electric field, still might induce tunneling transport (this should be a further work). On the basis of the observed behaviors, the features of carrier transport at contact/GaN interfaces can be summarized as follows: (1) carrier transport at the contact/GaN interface can be explained in terms of a barrier inhomogeneity model; (2) the tunneling probability E_{00} at the contact/GaN interface was consistent with the degree of potential fluctuation (V_{cp}); (3) on the basis of the relation $E_{00,NR} > E_{00,NF} > E_{00,GA}$, the largest tunneling probability of the NR samples is due to the combined effect of peculiar crystallographic structures and native defects; (4) indeed, according to the studies of Tung et al.[62] and Lucolano et al.,[57] the inhomogeneous Schottky barrier can be described using the "patch" model, where the local shallow barriers (or patches acting as the predominant conduction path) were embedded in a uniform higher Schottky barrier; (5) therefore, the current flow through patches will be influenced by the relative fraction of surrounding area with a higher barrier height; namely, the density and/or coverage ratio of patches will be a key parameter to the exact understanding of the Ohmic behaviors.

Now, it will be instructive to consider the way to obtain a reliable Ohmic contact to n-GaN. The formation of Ohmic contacts to the GA, NF, and NR samples is expected to be easy because of the strong carrier transport through the randomly distributed local shallow barriers acting as Ohmic patches. Accordingly, the TiN/Al/Ni/Au contacts formed on the GA, NF, and NR samples showed good Ohmic behavior with excellent linearity, as shown in Figure 7a, in which the size of the contact pads was 200 × 250 μm^2 and s = 20 μm. Another important contact issue reported by several groups is the thermal instability of the contact with the N-polar planes associated with the out-diffusion of Ga atoms. As shown in Figure 7b, however, thermal annealing performed at temperatures greater than 250 °C for 1 min in an N_2 ambient atmosphere led to an insignificant change in the $I-V$ curves of

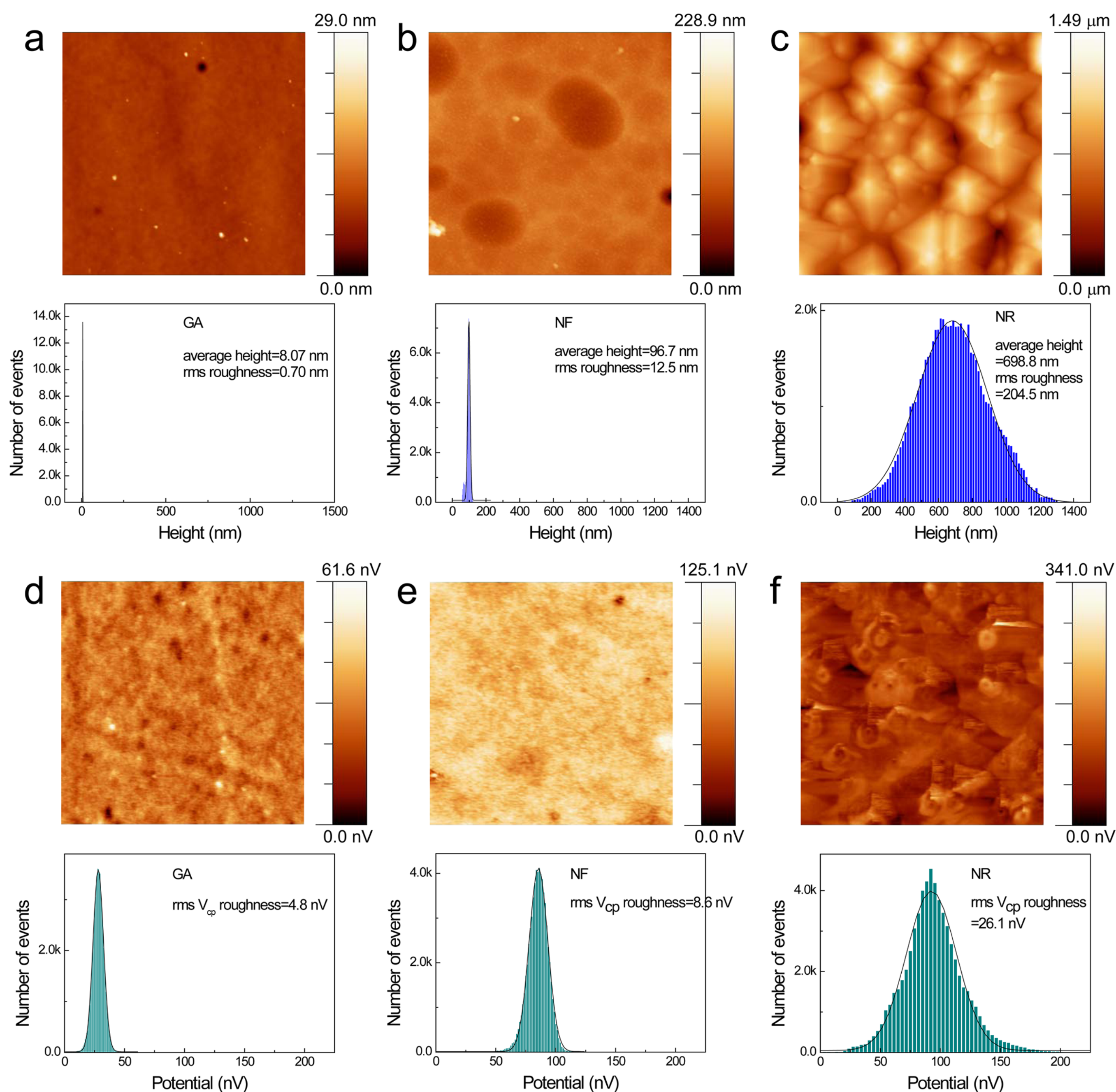

Figure 5. 5×5 μm^2 surface morphologies of the (a) GA, (b) NF, and (c) NR samples obtained by AFM and the corresponding surface contact potential (V_{cp}) images of the (d) GA, (e) NF, and (f) NR samples obtained by KPFM. The statistical distributions of feature height (obtained by AFM) and surface contact potential (obtained by KPFM) are also shown.

the NR samples; i.e., no thermal degradation occurred because of the successful suppression of out-diffusing Ga via the use of TiN barriers.[24] The same behavior was also observed in the NF samples (not shown). In addition, according to the area dependence of barrier height Φ_B (Figure 4b), the Ohmic contact is expected to degrade with the scaling down of the contact area. To address this issue, the area dependence of the Ohmic contact was also investigated for the NR sample, as shown in Figure 7c,d. Figure 7c shows the optical microscopy top views of TLM patterns with contact sizes of 200×250, 160×200, 100×80, 50×50, and 25×25 μm^2 (contact spacing s = 20, 60, and 150 μm). In Figure 7d, it is evident that the $I-V$ curves remained nearly linear with reduced contact size, even for the 25×25 μm^2 patterns. These results indicate that, as reported previously,[30] the TiN/Al scheme is very useful in the formation of a thermally stable Ohmic contact.

To investigate the thermal stability of vertical LEDs, the $I-V$ and optical output power−current ($L-I$) characteristics were compared before and after thermal annealing (250 °C for 10 min in an N_2 ambient atmosphere), as shown in Figure 8a. Here, note that the same TiN/Al/Ni/Au scheme was also used to form an n-type Ohmic contact on the wet-etched N-polar planes (NR) due to its guaranteed thermal stability. Unlike our expectation, however, the $L-I-V$ characteristics were significantly degraded after thermal annealing. For example, the $I-V$ curve showed leaky behavior, which resulted in a significant

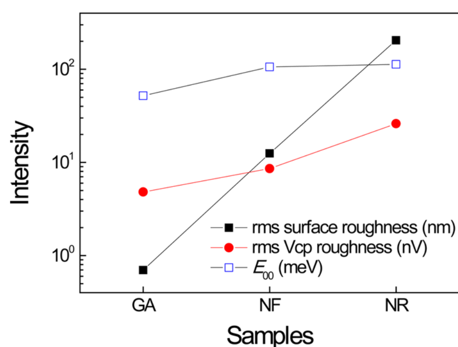

Figure 6. rms surface roughness, V_{cp} roughness, and E_{00} values of all samples.

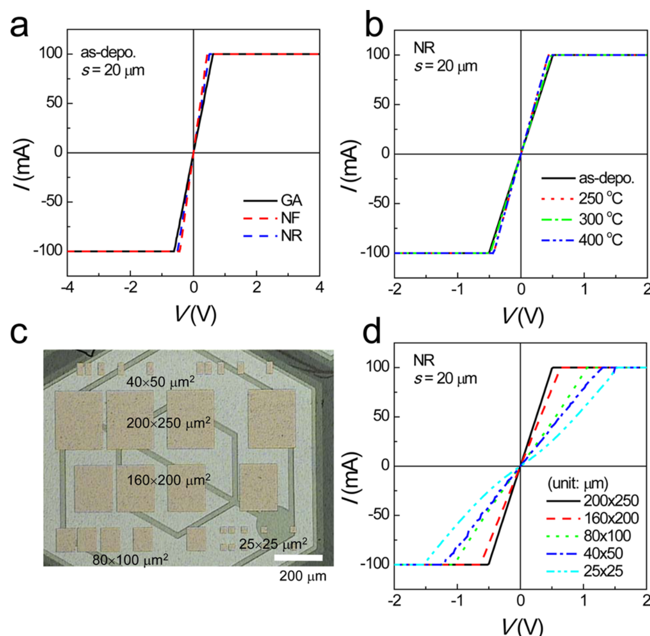

Figure 7. (a) $I-V$ curves of TiN/Al/Ni/Au contacts formed on the GA, NF, and NR samples, as measured from adjacent 200 × 250 μm^2 contact pads with s = 20 μm. (b) $I-V$ curves of the TiN/Al/Ni/Au contact formed on the NR sample as a function of the annealing temperature. (c) Optical microscopy top views of the TLM patterns. (d) $I-V$ curves of the TiN/Al/Ni/Au contact formed on the NR sample as a function of the contact size.

reduction in the optical output power. In addition, several $I-V$ sweeps even caused LED failure. This indicated that the vertical LEDs might be degraded during the packaging process because the performed annealing condition is comparable to that for packaging processes including die bonding and wiring. The inspection of electroluminescent (EL) images of the degraded LEDs revealed a clue for the degradation mechanism (see the inset of Figure 8a). For example, current crowding occurred near the probing n-contact pad, indicating that the current injection through the grid n-contact having a narrow contact width of ∼15 μm is very poor; i.e., the Ohmic contact formed on the small grid region was degraded. However, according to our experimental results shown in Figure 6, there was neither thermal degradation of the TiN/Al contact nor disruption of the Ohmic behavior with a reduction in the contact size.

To find the origin of the thermal instability of vertical LEDs, we tested the thermal stability of a contact with reduced contact size, as shown in Figure 8b. Unlike the nonannealed samples

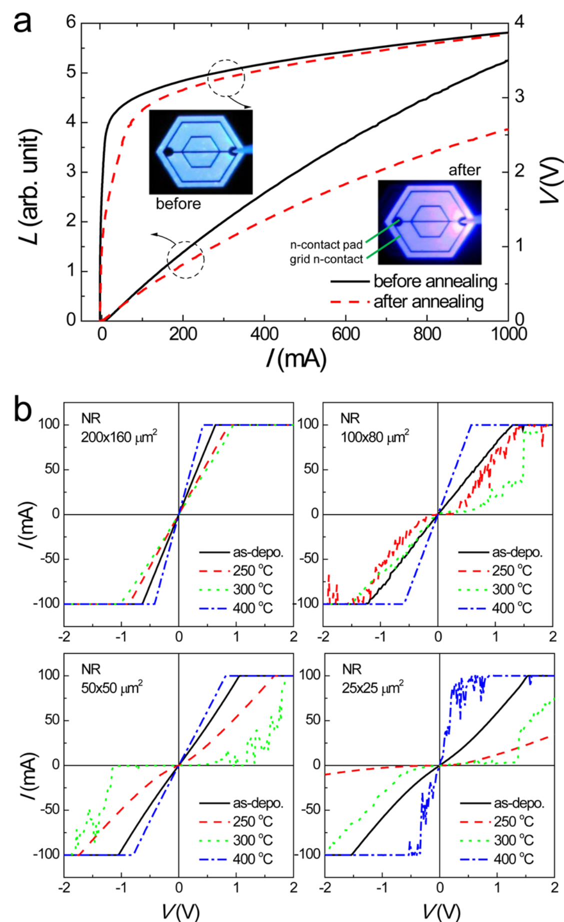

Figure 8. (a) $L-I-V$ characteristics of the vertical LEDs before and after thermal annealing at 300 °C for 10 min in an N_2 ambient atmosphere. The inset shows the EL images of LEDs measured at 350 mA. (b) $I-V$ curves of the TiN/Al/Ni/Au contacts formed on the NR samples with different contact sizes and annealing temperatures.

(see Figure 7d), the annealed NR samples showed significant $I-V$ degradation with decreased contact size, with critical contact dimensions of 100 × 80 μm^2. This indicated that the thermal instability of vertical LEDs is associated with thermal degradation of the n-contact at the grid region. This is plausible considering that, first, the Ohmic contact is mainly affected by the randomly distributed Ohmic patches, second, the absolute coverage area and/or number of Ohmic patches are much smaller in the narrow grid n-contact, and, third, the thermal stability of Ohmic patches is worse than that of the surrounding area with a higher barrier height and is statistically scattered. Indeed, the last hypothesis is also acceptable because the contact formed on defects would be thermally less stable because of the nature of the defects, i.e., a crystallographic imperfection with greater thermodynamic free energy, and the contact formed on the tip and/or edge of the hexagonal cone structure would be easily disrupted at elevated temperature (due to the structural unstable positioning).

To fabricate reliable vertical LEDs, therefore, it is proposed that the thermal instability of the n-contact formed on the small contact area should be improved. This can be achieved with the proper design of the n-contact; i.e., the use of a grid structure should be limited by enhancing the current spreading through the n-GaN layer (this will require an improvement in the epitaxial design and growth of the n-type channel layer), and

the n-contact dimension must be higher than the critical dimension. More essentially, to improve the thermal instability of the n-contact, the area dependence of the n-contact should be alleviated. This can be achieved if the origins of the barrier inhomogeneity are removed; namely, the crystallographic defects in the GaN films should be reduced in order to improve the thermal stability of the n-contact and ultimately the vertical LEDs. Last, it is also suggested that the high-temperature postannealing process be performed above 400 °C because most samples showed recovered $I-V$ curves after thermal annealing at 400 °C. This indicates that the Ohmic patches (contact formed on defects and/or specific cone structure) were degraded at the relatively low temperature range of ≤300 °C, while other factors began to improve the Ohmic contact at ≥400 °C. One possible cause of improved contact at the high annealing temperature is the formation of nitride phases (or generation of donor-like V_N) at the contact/GaN interface, resulting an increase of carrier concentrations. This is presently under investigation.

4. CONCLUSION

In summary, the carrier-transport behaviors of contacts formed on the GA, NF, and NR samples and their influence on the thermal instability of vertical LEDs were investigated. When the $I-V$ characteristics of Pd Schottky diodes and the KPFM images are compared, carrier transport at the contact/GaN interface could be reasonably explained in terms of the barrier inhomogeneity model, more specifically, barrier patch model; i.e., the local shallow barriers or patches acting as the predominant conduction path were embedded in a surrounding uniformly higher Schottky barrier. In this sense, on the basis of the observed contact degradation in the narrow area, the thermal instability of the Ohmic contact to the NR surface could be due to failure of the Ohmic patches, namely, disruption of the contacts formed on the defects and/or the tip/edge of the hexagonal cones, at elevated temperature. This indicates that thermally stable vertical LEDs can be obtained by eliminating small-area n-contacts and, more importantly, by reducing the origins of the Ohmic patches, namely, the crystallographic defects and geometrical surface structures.

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Notes

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